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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/644,735	08/21/2003	Myun-Joo Park	SEC.1067	6201
20987	7590	11/08/2006	EXAMINER PHAN, TRONG Q	
VOLENTINE FRANCOS, & WHITT PLLC ONE FREEDOM SQUARE 11951 FREEDOM DRIVE SUITE 1260 RESTON, VA 20190			ART UNIT 2827	PAPER NUMBER

DATE MAILED: 11/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/644,735	Applicant(s) PARK ET AL.	
	Examiner TRONG PHAN	Art Unit 2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 19 October 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,2,4-9,11-16 and 18-25 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,2,4-9,11-16 and 18-25 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-2, 4-9, 11-16 and 18-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuge, 6,466,496, in view of Ryan, 6,662,266, and Johnson et al., 6,233,650.

Kuge, 6,466,496, discloses in Fig. 3 a memory system comprising:

Regarding claims 1-2, 5-9, 13-16, 20-22 and 24:

system controller 1 which is read on the memory controller;

system data buses DQ each having a multi-bit structure (see lines 47, column 5) which may be a 32-bit (see lines 60, column 7), therefore, system data bus must inherently have a width of M bits where M can be a natural number or 32;

a plurality of memory modules groups 1000A, 1000B and 1000C... which can be divided into first through P-th memory module groups each group having N memory modules of two, for examples, group 1 (1000A and 1000B), group 2 (1000B and 1000C) and so on... ;

chip select signals /CS;

data buses between the memory modules are wired with the same length and the length of data transmission line/data transmission time can be made equal in

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compliance with JEDEC standard through line folding (see lines 23-29, column 3 and lines 66-67, column 5) which are read on the feature "wherein the N system data buses are wired such that data transmission times between the N memory modules within each of the first through P-th module groups and the memory controller are the same"

Regarding claims 4-5, 11-12 and 18-19:

as shown in Fig. 8, memory banks B0-B7;

Regarding claims 23 and 25:

as shown in Fig. 8, data input buffers 60 and 61 (see lines 1-11, column 8);

Regarding claims 1, 8 and 15:

Kuge, 6,466,496, discloses every feature as recited in claims 1-2, 4-9, 11-16 and 18-25 except the feature "each of the N system data buses having a width of M/N bits, where M is a natural number and N is a natural number greater than or equal to 2" and the feature "such that each of the N memory modules within each group is connected to a separate and distinct one of the N system data buses" as recited in claims 1, 8 and 15.

Ryan, 6,662,226, discloses in Fig. 1 the teaching of providing N 8-bit system data buses 106 each being connected to a separate and distinct one of the memory modules 108, 110, 112, 114, 116, 118, 120 and 122.

It would have been obvious under 35 USC 103(a) to one of ordinary skill in the art at time of the present invention to connect each of a plurality of memory modules groups 1000A, 1000B and 1000C...in Fig. 3 of Kuge, 6,466,496, to a separate and distinct one of the N system data bus as taught in Fig. 1 of Ryan, 6,662,226, for

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the purpose of accommodating the bus widths (see lines 29-34, column 1 of Ryan, 6,662,226).

Regarding claims 1, 8 and 15:

Kuge, 6,466,496, which is modified by Ryan, 6,662,226, disclose every feature as recited in claims -2, 4-9, 11-16 and 18-25 except the feature "the first through P-th memory module groups are operated in response to respective first through P-th chip select signals" as recited in claims 1, 8 and 15.

It should be noted that chip select signals /CS in Fig. 3 of Kuge, 6,466,496, can be divided into first through P-th chip select signals each including two chip select signals for selecting the two respective memory modules in each memory module group at the same time.

However, Johnson et al., 6,233,650, discloses in Fig. 1 the teaching of providing one chip select signal CS#4 as shown in Fig. 3A to a group of two memory modules 3 and 4 (see lines 35-39, column 4).

It would have been obvious under 35 USC 103(a) to one of ordinary skill in the art at time of the present invention was made to utilize the teaching of using one single chip select signal CS# 4 in Figs. 1 and 3A of Johnson et al., 6,233,650, for selecting the two respective memory modules 1000A and 1000B in each memory module group in Fig. 3 of Kuge, 6,466,496, which is modified by Ryan, 6,662,226, at the same time for the purpose of merely a matter of design choice for selecting two memory modules at the same time.

Conclusion

3. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Response to Arguments

4. Applicant's arguments filed on 10/19/06 have been fully considered and are persuasive. Therefore, the last Final office action of 7/31/06 has been withdrawn.

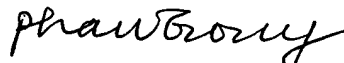
However, in view of Applicant's amendment, the newly discovered prior art of Ryan, 6,662,226, and upon further consideration, a new ground of rejection has been set forth and made **FINAL** as above.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **TRONG PHAN** whose telephone number is (571) 272-1794. The examiner can normally be reached on M-F (8:30-5:00).

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, AMIR ZARABIAN can be reached on (571)272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



**TRONG PHAN
PRIMARY EXAMINER**